HIGH EFFICIENCY, LOW ADJACENT CHANNEL LEAKAGE 2-V OPERATION GAAS POWER MESFET AMPLIFIER FOR 1.9-GHZ DIGITAL CORDLESS PHONE SYSTEM

M. Nagaoka, H. Wakimoto, K. Kawakyu, K. Nishihori, Y. Kitaura, T. Sasaki, A. Kameyama and N. Uchitomi

Toshiba R&D Center

1 Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 210, JAPAN

ABSTRUCT

A low-voltage GaAs power amplifier for 1.9-GHz digital mobile communication applications such as PHS handsets has been developed, using refractory WNx/W self-aligned gate MESFETs with p-pocket layers. This power amplifier operates with a single low 2-V supply, and an output power of 21.0 dBm, a power gain of 22.3 dB, a low dissipated current of 162.9 mA and a high power-added efficiency of 38.5 % were attained with a low 600-kHz adjacent channel leakage power of -58.0 dBc for 1.9-GHz π/4-shifted QPSK modulated input.

INTRODUCTION

Digital mobile communication has greatly expanded, such as the 1.9-GHz Japanese personal handy phone system (PHS) using π/4-shifted quadrature phase shift keying (QPSK) modulation. The PHS handset demands a enough linear transmission power amplifier, because the envelope of π/4-shifted QPSK modulated signal is not constant. It is specified that a PHS handset transmits a power of about 19dBm with adjacent channel leakage powers of less than -50 dBc and -55 dBc at 600 kHz and 900 kHz apart from 1.9 GHz, respectively. A 600-kHz adjacent channel leakage power of -58 dBc or below is required at 21-dBm output power for a transmission power amplifier, allowing for a sufficient margin in addition to losses inserted between the amplifier and the anttenna in the set. A GaAs MESFET is one of the best candidates for such application, because of its low signal distortion, low cost and good producibility.

There are evident needs for smaller size, longer talking and standby time, battery-driven mobile communication equipments. Negative voltage generation becomes a large obstacle to realize very compact handsets, because additional batteries or circuits such as dc-to-dc converters are necessary. There is a great need of a power amplifier which operates with a single voltage supply, as the other components in PHS handsets can operate without negative voltage. However, negative gate bias is necessary for most of conventional GaAs power MESFETs, with the exception of refractory WNx/W asymmetrically self-aligned gate power MESFETs with buried p-layers (BP-MESFETs), which were reported previously and can operate with a single voltage supply at 2.7 V[1,2].

Since battery size is the chief obstacle to the miniaturization of handsets, reduction of power dissipation results in great importance. As operation voltage is lowered, power dissipation for Si CMOS digital circuits such as base-band LSIs which are acting even in the standby mode of the set is reduced. Although present CMOS LSIs operate at about 3 V, lower-power CMOSs will be surely available in near future, which may operate with two Ni-H battery cells, for a 1.2-V Ni-H battery has recently had almost the same volume energy density as a Li ion battery. To our knowledge, however, no GaAs power MESFET amplifier which operates with high efficiency and low adjacent channel leakage power at about 2 V has been reported yet. In general, lowering supply voltage causes both poorer linearity and efficiency for conventional power amplifiers.

This paper describes a GaAs power amplifier using refractory WNx/W self-aligned gate MESFETs with p-pocket layers (p-pocket MESFETs)[3], which we newly developed, succeeding asymmetrically self-aligned BP-MESFETs. This power amplifier operates with high efficiency and low adjacent channel leakage power with a single low 2-V supply.

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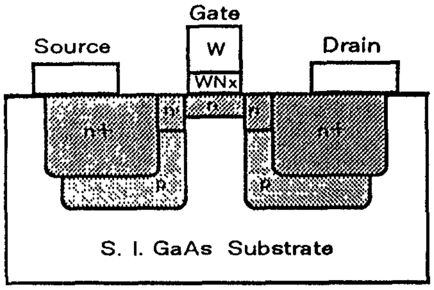

Figure 1: Cross-sectional view of self-aligned gate GaAs MESFET with p-pocket layers

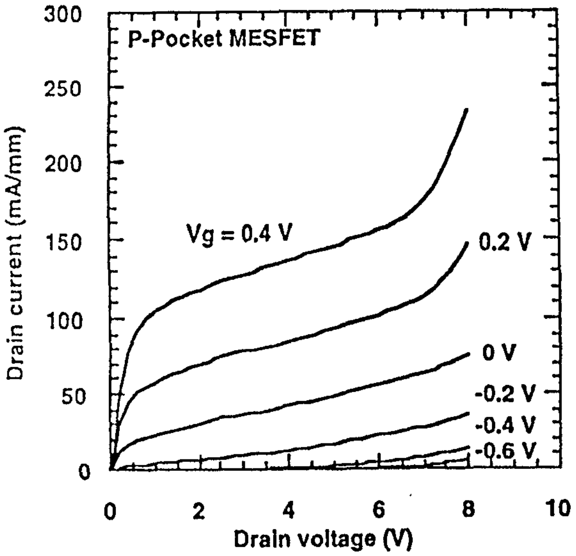

Figure 2: Typical I-V characteristics of p-pocket MESFET

FET STRUCTURE AND PERFORMANCE

Refractory gate technology is a promising approach for power MESFET production because of its simple process, good device reproducibility and reliability. Figure 1 shows a typical schematic cross-sectional view of a self-aligned gate GaAs MESFET with p-pocket layers. This MESFET is fabricated on a semi-insulating GaAs substrate through fully ion-imlantation process and it has a planar self-alignment structure, including p-pocket layers not under the channel but exclusively under the source and drain regions, to eliminate the short channel effect. These p-layers which are formed by

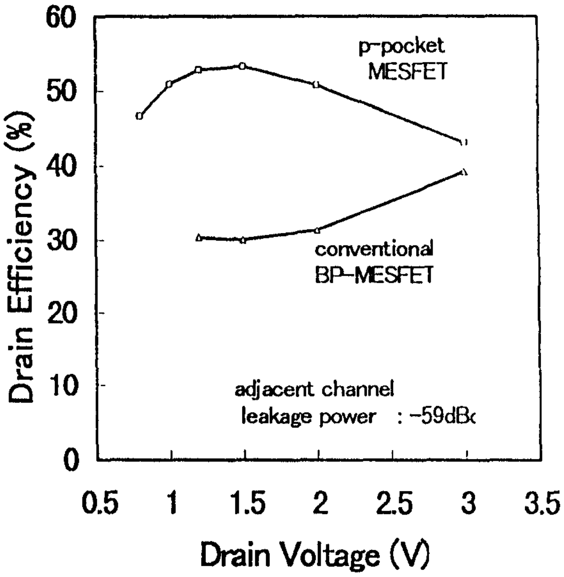

Figure 3: Voltage dependence of drain efficiency of p-pocket power MESFET, compared with conventional power BP-MESFET

Mg ion implantation self-aligned against the gate electrode are completely depleted to avoid excess parasitic capacitance. The sputter-deposited WNx/W bilayer is employed for reducing gate resistance to 1/20, compared with a WNx monolayer[4]. The gate length is 0.8μm.

For low-voltage, low-distortion, high-efficiency operation of power MESFETs, both low on-state resistance and sufficiently little change of drain conductance are quite desirable. In addition, high transconductance is really essential to single voltage supply operation of power MESFETs, because of small gate input voltage swing which is determined fundamentally by Schottky barrier height and gate bias. Figure 2 shows the typical drain I-V characteristics of the p-pocket MESFET. Holes are generated by impact ionization, especially in higher drain bias conditions. In the case of the p-pocket MESFET, few of them are distributed under the channel but in the source-side p-pocket region, and therefore, anomalous increase of drain current against drain voltage, so-called "I-V kink", has never appeared, which is different from the case of the conventional BP-MESFET, where holes are collected in the buried p-layer under the channel. In addition, self-alignment structure realizes both low on-state resistance and high transconductance. These good features realized a high drain efficiency over 50 % and a low 600-kHz adjacent channel leakage power for 1.9-GHz π/4-shifted QPSK modulated input even at 2-V drain bias

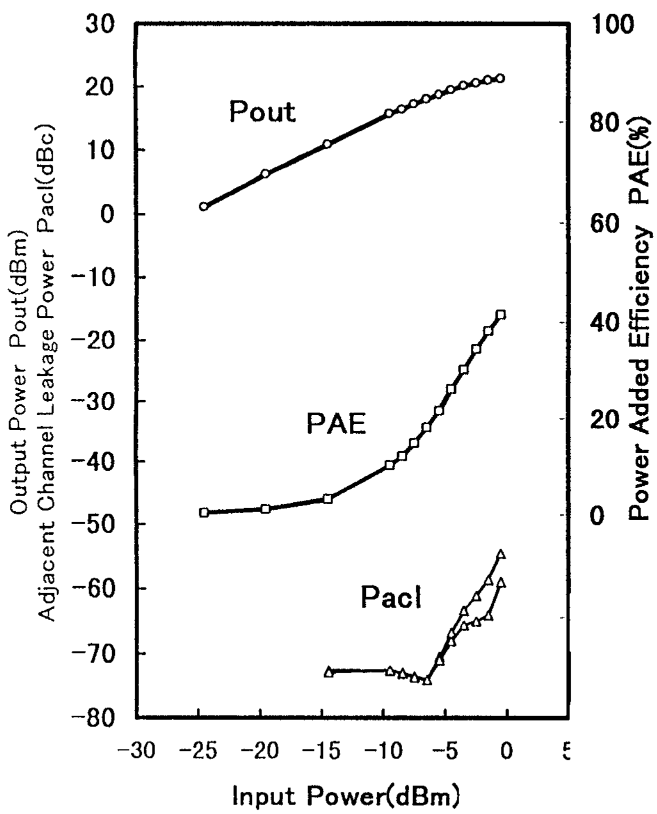

Figure 4: Output power characteristics of power amplifier for 1.9-GHz π/4-shifted QPSK modulated input with a single 2-V supply

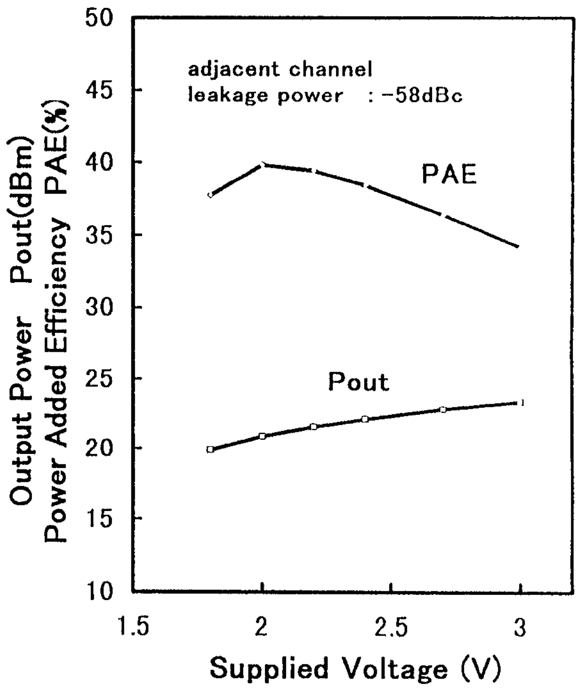

Figure 5: Voltage dependence of output power and power-added efficiency of power amplifier

under a non-negative gate bias condition. As a measured example, voltage dependence of drain efficiency of a p-pocket power MESFET, compared with that of an asymmetrically self-aligned power BP-MESFET, under a 600-kHz adjacent channel leakage power of -59dBc, is shown in Fig. 3. As supplied voltage was lowered, drain efficiency decreased in the BP-MESFET. As for the p-pocket MESFET, contrastively, higher drain efficiency at 2 V or below was obtained than 43% at 3 V. Though p-pocket power MESFETs are enough useful for conventional 3-V PHS handsets, they are more suitable for lower voltage applications.

AMPLIFIER DESIGN AND PERFORMANCE

A two-stage power MESFET amplifier was designed. The GaAs power amplifier chip contains two p-pocket MESFETs and an interstage circuit which is composed of a Au-plated spiral inductor, a MIM capacitor, and bulk resistors. Input, output, and biasing circuits were designed on an aluminum module substrate, in order not only to minimize the chip area and reduce the bias voltage drop, but also to reduce the transmission loss of the output matching circuit with low impedance, for lower voltage operation necessitates larger output current swing. The chip size is as small as 1.0 mm x 1.0 mm. Load impedance for the power MESFET in the second-stage was determined by load-pull measurement using a 1.9-GHz π/4-shifted QPSK modulated source.

Output power performance of the GaAs power amplifier for 1.9-GHz π/4-shifted QPSK modulated input was measured with a single 2 V supply. Figure 4 shows the typical output power characteristics under a condition that gate biases of the first and second stage FETs were 0 V and 0.08 V, respectively. An output power of 21.0 dBm and a power gain of 22.3 dB were measured, where adjacent channel leakage power was as low as -58.0 dBc at 600 kHz apart from 1.9 GHz. A low dissipated current of 162.9 mA and a high power-added efficiency of 38.5 % were attained. Thus the power amplifier operates with sufficiently low distortion and low power dissipation even at 2 V in PHS. Figure 5 shows voltage dependence of output power and power added efficiency of this power amplifier at a 600-kHz adjacent channel leakage power of -58 dBc. The highest power added efficiency was obtained at 2 V, although output power decreased monotonously with lowering supplied voltage.

CONCLUSION

A GaAs power amplifier has been developed using refractory WNx/W self-aligned gate MESFETs with p-pocket layers. This power amplifier can operate with a single low 2-V supply, and an output power of 21.0 dBm, a low dissipated current of 162.9 mA and a high power-added efficiency of 38.5 % were attained with a low 600-kHz adjacent channel leakage power of -58.0 dBc in 1.9-GHz $\pi/4$-shifted QPSK modulation. The GaAs power amplifier using the p-pocket MESFETs is quite promising for use in near-future low-voltage and low-power digital mobile communication applications.

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